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APPLICATION

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TITLE: IMAGE SENSOR WITH PIXELS HAVING MULTIPLE CAPACITIVE STORAGE ELEMENTS

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IMAGE SENSOR WITH PIXELS HAVING MULTIPLE CAPACITIVE STORAGE ELEMENTS

BACKGROUND

The present invention relates to image sensors with pixels having multiple capacitive storage elements.

Image sensors can be used in a wide variety of fields, including machine vision, robotics, guidance and navigation, automotive applications, and consumer products. They can include on-chip circuitry that controls image sensor operation, signal read-out and image processing functions. Image sensors can utilize, for example, active pixel sensor (APS) technology with each active pixel sensor including one or more active transistors. Each pixel sensor element can provide an output value that represents a particular portion of an image.

SUMMARY

An apparatus, such as an imager, includes a pixel that has (i) a buffer transistor having an input, (ii) first and second capacitive storage elements each of which selectively can be coupled to the input of the buffer transistor, and (iii) a photosensitive element having an output which selectively can be coupled to the input of the buffer transistor. The apparatus also includes a readout circuit that selectively can be coupled to an output of the buffer transistor.

A first signal level, sensed by the photosensitive element, can be stored by the first capacitive storage element, and a second signal level, sensed by the photosensitive

element, can be stored by the second capacitive storage element. The first and second signal levels can be read out from the pixel.

In various implementations, the apparatus may include one or more of the following features. A first switch can be coupled between the output of the photosensitive element and the input of the buffer transistor. A second switch can be coupled between the first capacitive storage element and the input of the buffer transistor, and a third switch can be coupled between the second capacitive storage element and the input of the buffer transistor. A fourth switch can be coupled between a power supply node and the input of the buffer transistor. Each of the switches can be selectively operable in an open or closed state.

A controller can provide signals to control the respective states of the first, second, third and fourth switches. The controller can be configured to provide signals to cause the first capacitive storage element to store a first signal level sensed by the photosensitive element during a first integration time and to cause the second capacitive element to store a second signal level sensed by the photosensitive element during a second integration time. For example, the controller can be configured to provide signals to cause (i) the first and second switches to be closed during the first integration time, (ii) the third and fourth switches to be open during the first integration time, (iii) the first and third switches to be closed during the second integration time, and (iv) the second and fourth switches to be open during the second integration time.

The controller also can be configured to provide signals to reset the photosensitive element and the first capacitive storage element prior to the first integration period and to reset the photosensitive element and the second capacitive storage element prior to the

second integration period. For example, the controller can be configured to provide signals to cause (i) the first, second and fourth switches to be closed just prior to the first integration period, and (ii) the first, third and fourth switches to be closed just prior to the second integration period.

The controller can be configured for providing signals to selectively transfer the first signal level from the first capacitive storage element to the readout circuit and to transfer the second signal level from the second capacitive element to the readout circuit. Furthermore, the controller can be configured to provide signals to reset the input of the buffer transistor prior to transferring the first signal level from the first capacitive storage element to the readout circuit and to reset the input of the buffer transistor prior to transferring the second signal level from the second capacitive storage element to the readout circuit. Thus, the controller can be configured to provide signals to cause the fourth switch to be closed prior to transferring the first signal level from the first capacitive storage element to the readout circuit and to cause the fourth switch to be closed just prior to transferring the second signal level from the second capacitive storage element to the readout circuit.

In some implementations, the reset switch is configured for operation in a sub-threshold reset mode.

An integrated circuit can include an array of pixels each of which includes multiple capacitive storage elements. Readout circuitry selectively can be coupled to outputs of buffer transistors of selected pixels in the array. The pixels, as well as the controller and the readout circuitry, can be formed as part of a monolithic integrated circuit.

One or more of the following advantages may be present in some implementations. Signals representing the difference between two exposures can be obtained without measuring pixel reset values. Eliminating measurement of pixel reset levels can help reduce the noise that is inherent in such measurements. Additional reductions in thermal or "kTC" noise can be achieved by operating the reset switch in sub-threshold mode.

Other features and advantages will be readily apparent from the following detailed description, the accompanying drawings and the claims.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a system block diagram of an integrated circuit chip.

FIG. 2 illustrates further details of the integrated circuit chip.

FIG. 3 is a schematic diagram of a pixel and an associated column readout circuit.

FIG. 4 is a timing diagram of signals associated with FIG. 3.

FIG. 5 is a schematic diagram of a pixel.

DETAILED DESCRIPTION

As shown in FIG. 1, a monolithic integrated imaging circuit chip 10 includes an array of active pixel sensors 30 and a controller 32 that provides timing and control signals to control operation of the pixels and enable reading out of signals stored in the pixels. The array 30 may have dimensions of 128 by 128 pixels or 256 by 256 pixels, although, in general, the size of the array will depend on the particular implementation.

The imager can be read out a row at a time using a parallel column readout architecture. The controller 32 selects a particular row of pixels in the array 30 by controlling the operation of a vertical addressing circuit 34 and row drivers 40. Charge signals stored in the selected row of pixels are transferred to a readout circuit 42. The pixels read from each of the columns then can be read out sequentially using a horizontal addressing circuit 44. A differential signal for each pixel can be provided at an output of the readout circuit 42.

As shown in FIG. 2, the array 30 includes multiple columns 49 of active pixel sensors 50. Each column includes multiple rows of sensors 50. Signals from the active pixel sensors 50 in a particular column can be read out to a readout circuit 52 associated with that column. For example, pixel signal levels corresponding to different exposure times may be stored by the readout circuit 52 and then transferred to a common output stage 54 over lines 70, 72. The output stage 54 can provide a differential signal corresponding to the difference between the pixel signals obtained during the different exposure times.

As shown in FIG. 3, a single CMOS active pixel sensor 50 includes a photo-sensitive element 60 buffered by a source-follower transistor M1. The source-follower transistor M1 is coupled to a power supply voltage (vdd) and to a row selection switch which can be implemented by a transistor M2. A signal (ROW) is applied to the gate of the row selection transistor M2 to enable reading out of signals from a pixel in the selected row. The row selection signal (ROW) is common to an entire row of pixels. In one implementation, the photosensitive element 60 includes a photogate. A floating diffusion node 62 that serves as a sense node is coupled to the gate of the source-follower

M1 and is separated from the photosensitive element 60 by a transfer gate S1. The pixel 50 includes a reset switch S4 that can be implemented as a transistor. When the reset switch S4 is closed, it is coupled to a power supply voltage (Vrst).

The pixel includes storage capacitors C1, C2 for storing charge or voltage signals corresponding to optical signals sensed by the photosensitive element 60. Respective switches S2, S3, which can be implemented as transistors, are coupled between the floating diffusion node 62 and the capacitors C1, C2. The values of the capacitors C1, C2 should be substantially the same.

As illustrated by FIG. 3, output signals from a pixel 50 can be provided to the readout circuit 52 through a bus 64 that is common to an entire column 49 of pixels. The readout includes a load transistor M5 and two sample and hold switches M3, M4, which can be implemented as transistors. The switch M3 is controlled by a signal (SHS) applied to its gate, whereas the switch M4 is controlled by a signal (SHR). When a sample and hold switch is closed, a voltage signal that is present on the common pixel output bus 64 is stored by the corresponding capacitor. For example, when the switch M3 is closed, a voltage signal that is present on the bus 64 is stored by the capacitor C3. Similarly, when the switch M4 is closed, a voltage signal that is present on the bus 64 is stored by the capacitor C4.

Signals for controlling the state of the various switches are provided by the controller 32. For purposes of the following discussion, it is assumed that each switch is implemented as an n-type metal oxide semiconductor (NMOS) transistor switch such that the switch is open when its control signal is high and is closed when its control signal is low. The reverse is applicable to p-type MOS (PMOS) switches.

In operation, the photosensitive element 60 and the first storage capacitor C1 are reset by closing and subsequently opening the reset switch S4 while the switches S1 and S2 are closed. As shown, for example, in FIG. 4, the reset switch S4 is closed at time t_1 and subsequently opened at time t_2. Switches S1 and S2 remain closed to integrate photocharge on the first capacitor C1 during a first integration period. The first integration period ends at time t_3 when the switches S1 and S2 are closed. Next, the photosensitive element 60 and the second storage capacitor C2 are reset by closing and subsequently opening the reset switch S4 while the switches S1 and S3 are opened. As shown in FIG. 4, the reset switch S4 is closed at time t_4 and subsequently opened at time t_5. Switches S1 and S3 remain closed to integrate photocharge on the first capacitor C2 during a second integration period. The second integration period ends at time t_6 when the switches S1 and S3 are opened. The first and second integration periods correspond to first and second exposure periods, respectively. The imager can be operated in shutter mode with common integration periods for the entire array of pixels.

After completion of the two exposure periods, the row selection signal (ROW) enables (at time t_7) a pixel in the selected row to be coupled electrically to the column bus 64. The pixel's floating node 62 is reset by closing reset switch S4 at time t_8. After re-opening switch S4 (at time t_9), the signal stored by the first capacitor C1 is transferred to the source follower M1 by closing the switch S2 (at time t_{10}). The pixel signal corresponding to the first exposure time passes through the row selection switch M2 to the bus 64. The sample and hold switch M3 also is enabled at time t_{10}, thereby allowing the pixel signal for the first exposure time to be sampled and stored by the capacitor C3. At time t_{11}, the switch S2 and the switch M3 are opened.

The pixel's floating node 62 again is rest by closing reset switch S4 at time t_{12}. After re-opening switch S4 (at time t_{13}), the signal stored by the first capacitor C2 is transferred to the source follower M1 by closing the switch S3 (at time t_{14}). The pixel signal corresponding to the second exposure time passes through the row selection switch M2 to the bus 64. The sample and hold switch M4 also is enabled at time t_{14}, thereby allowing the pixel signal for the second exposure time to be sampled and stored by the capacitor C4. At time t_{15}, the switch S3 and the switch M4 are opened.

The signals stored by the capacitors C3 and C4 can be read out, respectively, through lines 70, 72 to the output stage 54 which includes circuitry for determining the difference between the input signals. Thus, the output signals from stage 54 represent the difference between the images sensed and stored by the pixel during the two exposure times. The output signals can be converted to corresponding digital signals using an analog-to-digital converter (ADC). The signals from the other pixels in the selected row can be read out sequentially. Alternatively, a separate output stage 54 and ADC can be provided for each column or block of columns to provide parallel readout.

After processing the signals from the pixels in the selected row, another row of pixels can be selected to allow the stored signal levels to be read out and processed.

One advantage that may be achieved through the foregoing technique is the ability to obtain differential values representing the difference between two exposures without measuring pixel reset values. Eliminating measurement of pixel reset levels can help reduce the noise that is inherent in such measurements. Nevertheless, the pixel design described above also can be used to obtain differential values representing the difference between the pixel signal level and pixel reset level.

Additional reductions in thermal or "kTC" noise can be achieved by operating the reset switch S4 in soft, or sub-threshold, reset mode. In that case, as illustrated in FIG. 5, the switch S4 should be implemented as an NMOS transistor, whereas the switches S1, S2 and S3 should be implemented as PMOS transistors operating in linear triode mode to ensure complete transfer of signals between the photosensitive element 60, the capacitive storage memories C1 and C2, and the source follower M1.

Other implementations are within the scope of the claims.